MEG 01-015

REMARKS

This is a full and timely response to the Office Action mailed Dec. 8, 2005. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

1.Present Status of the Application

Upon entry of the amendments in this response, claims 242-244 remain pending in the present application. More specifically, claims 242-244 are currently amended; and claims 1-241 are canceled without prejudice, waiver, or disclaimer. These amendments are specifically described above. It is believed that the amendments add no new matter to the present application.

2.Response To Objections/Rejections

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response To Claim 242

As currently amended, independent claim 242 is recited below:

242. A chip packaging method comprising:
joining a die and a substrate;
after said joining said die and said substrate, depositing a passive device over said substrate, wherein said passive device has a portion not over said die; and
separating said substrate.

MEG 01-015

Section I

Reconsideration of Claim 242 rejected under 35 U.S.C. 102(e) as being anticipated by US2002/0,074,641 to Towle et al.

Applicants respectfully assert that the chip packaging method claimed in claim 242 patentably distinguishes over the citation by Towle et al (US2002/0074641).

Towle et al teach that a chip packaging method comprises joining a die 214 or 314 and a substrate 202 or 302, depositing multiple metal layers and multiple dielectric layers over the substrate 202 or 302, and separating the substrate 202 or 302, wherein the metal layers are separated by the dielectric layers. ~ *See FIGS. 11-17 and 30-34* ~ Even though the capacitance can be produced by the dielectric layer between the metal layers, Towle et al fail to teach the capacitance is provided by a capacitor for a specific usage. The dielectric layer between the metal layers has the nature required to produce capacitance, which is a natural phenomenon that is not required to be invented or thought of by a human. However, the structure of the dielectric layer between the metal layers used for a capacitor is required to be invented or conceived by a human. Towle et al fail to teach the structure of the dielectric layer between the metal layers can be used as a capacitor, a kind of passive device, for a specific usage. Therefore, applicants respectfully do not think the chip packaging method as claimed in claim 242, as a whole, is taught by Towle et al.

For at least the foregoing reasons, applicants respectfully submit independent claim 242 patently distinguishes over the prior art references, and should be allowed.

Section II

Reconsideration of Claim 242 rejected under 35 U.S.C. 102(e) as being anticipated by US6,867,499 to Tabrizi.

Applicants respectfully assert that the chip packaging method claimed in claim 242 patentably distinguishes over the citation by Tabrizi (US6,867,499).

Tabrizi teaches that a chip packaging method comprises joining a die 520 and a substrate 510, depositing a metal layer 560 over the substrate 510 and die 520, and separating the substrate 510. ~ *See FIG. 5 and lines 9-13, col. 4* ~ Tabrizi teaches that a passive device may be added on the metal layer 560, but fails to teach that the passive device is added on the metal layer 560 over the die 520 or on the metal layer 560 not over the die 520. Therefore, applicants respectfully do not think the chip packaging method as claimed in claim 242, as a whole, is taught by Tabrizi.

For at least the foregoing reasons, applicants respectfully submit independent claim 242 patently distinguishes over the prior art references, and should be allowed.

MEG 01-015
Response To Claim 243

As currently amended, independent claim 243 is recited below:

243. A chip packaging method comprising:
joining a die and a substrate;
after said joining said die and said substrate, depositing a passive device over said substrate, wherein said passive device has a first end connected down to said die and a second end connected to a topmost pad of said chip package; and
separating said substrate.

Section I

Reconsideration of Claim 243 rejected under 35 U.S.C. 102(e) as being anticipated by US2002/0,074,641 to Towle et al.

Applicants respectfully assert that the chip packaging method claimed in claim 243 patentably distinguishes over the citation by Towle et al (US2002/0074641).

Towle et al teach that a chip packaging method comprises joining a die 214 or 314 and a substrate 202 or 302, depositing multiple metal layers and multiple dielectric layers over the substrate 202 or 302, and separating the substrate 202 or 302, wherein the metal layers are separated by the dielectric layers. ~ *See FIGS. 11-17 and 30-34* ~ Even though the capacitance can be produced by the dielectric layer between the metal layers, Towle et al fail to teach the capacitance is provided by a capacitor for a specific usage. The dielectric layer between the

metal layers has the nature required to produce capacitance, which is a natural phenomenon that is not required to be invented or thought of by a human. However, the structure of the dielectric layer between the metal layers used for a capacitor is required to be invented or conceived by a human. Towle et al fail to teach the structure of the dielectric layer between the metal layers can be used as a capacitor, a kind of passive device, for a specific usage. Therefore, applicants respectfully do not think the chip packaging method as claimed in claim 243, as a whole, is taught by Towle et al.

For at least the foregoing reasons, applicants respectfully submit independent claim 243 patently distinguishes over the prior art references, and should be allowed.

Section II

Reconsideration of Claim 243 rejected under 35 U.S.C. 102(e) as being anticipated by US6,867,499 to Tabrizi.

Applicants respectfully assert that the chip packaging method claimed in claim 243 patentably distinguishes over the citation by Tabrizi (US6,867,499).

Tabrizi teaches that a chip packaging method comprises joining a die 520 and a substrate 510, depositing a metal layer 560 over the substrate 510 and die 520, and separating the substrate 510. *~See FIG. 5 and lines 9-13, col. 4~* Tabrizi teaches that a passive device may be added on

the metal layer 560, but fails to teach that the passive device has a first end connected down to the die 520 and a second end connected to a topmost pad of the chip package. Therefore, applicants respectfully do not think the chip packaging method as claimed in claim 243, as a whole, is taught by Tabrizi.

For at least the foregoing reasons, applicants respectfully submit independent claim 243 patently distinguishes over the prior art references, and should be allowed.

Response To Claim 244

As currently amended, independent claim 244 is recited below:

244. A chip packaging method comprising:
providing a die having a top surface at a horizontal level;
depositing a passive device over said horizontal level, wherein said passive device has a portion not over said die; and
depositing a trace over said horizontal level, wherein said trace has a portion not over said die.

Section I

Reconsideration of Claim 244 rejected under 35 U.S.C. 102(e) as being anticipated by US2002/0,074,641 to Towle et al.

Applicants respectfully assert that the chip packaging method claimed in claim 244 patentably distinguishes over the citation by Towle et al (US2002/0074641).

Towle et al teach that a chip packaging method comprises providing a die 214 or 314 having a top surface at a horizontal level, and depositing multiple metal layers and multiple dielectric layers over the horizontal level, wherein the metal layers have a portion not over the die 214 or 314. ~ *See FIGS. 11-17 and 30-34* ~ Even though the capacitance can be produced by the dielectric layer between the metal layers, Towle et al fail to teach the capacitance is provided by a capacitor for a specific usage. The dielectric layer between the metal layers has the nature required to produce capacitance, which is a natural phenomenon that is not required to be invented or thought of by a human. However, the structure of the dielectric layer between the metal layers used for a capacitor is required to be invented or conceived by a human. Towle et al fail to teach the structure of the dielectric layer between the metal layers can be used as a capacitor, a kind of passive device, for a specific usage. Therefore, applicants respectfully do not think the chip packaging method as claimed in claim 244, as a whole, is taught by Towle et al.

For at least the foregoing reasons, applicants respectfully submit independent claim 244 patently distinguishes over the prior art references, and should be allowed.

Section II

MEG 01-015

Reconsideration of Claim 244 rejected under 35 U.S.C. 102(e) as being anticipated by US6,867,499 to Tabrizi.

Applicants respectfully assert that the chip packaging method claimed in claim 244 patentably distinguishes over the citation by Tabrizi (US6,867,499).

Tabrizi teaches that a chip packaging method comprises providing a die 520 having a top surface at a horizontal level, and depositing a metal layer 560 over the horizontal level. ~ *See FIG. 5 and lines 9-13, col. 4* ~ Tabrizi teaches that a passive device may be added on the metal layer 560, but fails to teach that the passive device is added on the metal layer 560 over the die 520 or on the metal layer 560 not over the die 520. Therefore, applicants respectfully do not think the chip packaging method as claimed in claim 244, as a whole, is taught by Tabrizi.

For at least the foregoing reasons, applicants respectfully submit independent claim 244 patently distinguishes over the prior art references, and should be allowed.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

MEG 01-015

Date : 2/20/2006

Respectfully submitted,

Mou-Shiung Lin, CEO
For and on behalf of MEGIC